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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Eric NEYRET et al.

Confirmation No.: 1950

Patent No.: 6,939,783 B2

Application No.: 10/784,040

Patent Date: September 6, 2005

Filing Date: February 20, 2004

For: PREVENTIVE TREATMENT METHOD FOR A MULTILAYER SEMICONDUCTOR WAFER

Attorney Docket No.: 4717-10100

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 C.F.R. § 1.322

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Patentees hereby respectfully request the issuance of a Certificate of Correction in connection with the above-identified patent. The corrections are listed on the attached Form PTO-1050. The corrections requested are as follows:

Column 6, line 10 (claim 1, line 9), after "the subsequent treatment, wherein the", change "multilaver" to -- multilayer --. Support for this change appears in application claim 1 as amended on April 18, 2005.

Column 7, line 9 (claim 14, last line), after "for a time of about 1 to 5", change "minute" to -- minutes --. Support for this change appears in application claim 16.

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The requested corrections are for errors that appear to have been made by the Office. Therefore, no fee is believed to be due for this request. Should any fees be required, however, please charge such fees to Winston & Strawn LLP Deposit Account No. 50-1814. Please issue a Certificate of Correction in due course.

Respectfully submitted,

9/20/05
Date

Allan A. Fanucci, Reg. No. 30,256

WINSTON & STRAWN LLP
Customer No. 28765

212-294-3311

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 6,939,783 B2
DATED: September 6, 2005
INVENTORS: Neyret et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 6:
Line 10, after "the subsequent treatment, wherein the", change "multilaver" to -- multilayer --.

Column 7:
Line 9, after "for a time of about 1 to 5", change "minute" to -- minutes --.

late the peripheral edge of the exposed intermediate layer. It has been observed that RTA causes a beneficial effect in the exposed intermediate layer. In particular, the RTA process can make the surface layer of the wafer "drop off" (in the case of an SOI wafer, the layer **101** shown in FIG. **1** corresponds to a layer of monocrystalline silicon). This surface layer also overlaps and encapsulates the periphery of the intermediate layer (layer **102** in FIG. **1**) that was previously exposed. FIG. **4** illustrates this overlapping and encapsulation effect. In particular, FIG. **4** illustrates the case of an SOI wafer that had been exposed to a stabox step and then exposed to RTA. These steps carried out in this order results in stabilizing the bonding interface between the receiving substrate (layer **103**) and the donor substrate (layers **101** and **102**). As shown in FIG. **4**, the intermediate layer **102** is entirely encapsulated by the surface layer **101**. The layer **102** is thus protected from subsequent heat treatments that may be applied to the wafer.

The RTA is carried out at a high temperature for a short period. When an SOI wafer is treated, the heat treatment may be carried out at a temperature on the order of about 1150° C. to 1300° C. and preferably 1200° C. for a period of between about 1 and 5 minutes and preferably less than about 3 minutes. This RTA is preferably carried out in a hydrogen and/or argon atmosphere.

The RTA can also be done immediately after the wafer has been detached. In this case, the bonding interface between the layer **103** and the rest of the wafer had not been stabilized by a heat treatment. But tests have demonstrated that this embodiment can also be used to overlap and encapsulate the intermediate layer without degrading the bonding interface. FIG. **5** is an illustration of this embodiment of the invention. (The edge in FIG. **5** represents the "right" edge of the wafer, while the "left" edge of the wafer is shown in the other figures.)

Referring to FIG. **5**, the surface layer **101** overlaps and encapsulates the intermediate layer **102** so that it is protected from subsequent treatments. It should also be noted that the RTA has not degraded the bonding interface between layers **102** and **103**. The RTA can thus be used immediately after the wafer has been detached, or during a subsequent step such as after a stabox step (see FIG. **4**). In general, use of RTA is a means of securing the intermediate layer for subsequent heat treatment steps that may be applied to the wafer.

It should be noted that the present method can be applied to wafers other than SOI wafers. It is also possible to overlap and encapsulate several intermediate layers in the wafer instead of a single layer.

In general, the present technique causes overlapping and encapsulation of a surface region of the wafer by a layer of material. In particular, this layer of material may come from the surface layer of the wafer, as shown in the present examples illustrated above. In all of the embodiments, the RTA protects the intermediate layer of the wafer so that it is then possible to apply subsequent treatments like those mentioned above to the wafer. In particular, a wafer treated according to the present method can be subjected to a prolonged high temperature heat treatment without degrading the intermediate layer. However, note that in this case, a polishing step (such as CMP) should not be conducted between the use of RTA and the prolonged high temperature heat treatment. The polishing step under these circumstances would at least partially destroy the protection accorded the intermediate layer by the present method, so that a prolonged high temperature heat treatment could degrade the intermediate layer.

What is claimed is:

1. A preventive treatment method for a multilayer semiconductor wafer that includes a supporting substrate, at least one intermediate layer and a surface layer in which an intermediate layer has an exposed lateral edge and the wafer is to be subjected to a subsequent treatment, which method comprises treating the wafer to cause a portion of the surface layer to encapsulate the exposed lateral edge of the intermediate layer to prevent attack on the peripheral edge during the subsequent treatment, wherein the multilayer semiconductor wafer is formed by transferring at least the surface layer from a donor wafer to at least one intermediate layer by a layer transfer technique.

2. The method of claim **1** wherein the treating comprises annealing the wafer by heating to a temperature and for a time sufficient to cause the surface layer portion to cover the exposed lateral edge of the intermediate layer.

3. The method of claim **1** wherein the multilayer semiconductor wafer has a silicon on insulator structure.

4. The method of claim **1** wherein the surface layer is transferred by forming a zone of weakness in the donor wafer at a depth sufficient to define the surface layer, bonding the surface layer of the donor wafer to the intermediate layer of the supporting substrate and then detaching the surface layer from the donor wafer.

5. The method of claim **4** wherein the zone of weakness is formed by implanting ions into the donor wafer.

6. The method of claim **1** which further comprises subjecting the wafer to the subsequent treatment without detrimentally affecting the edge of the intermediate layer.

7. The method of claim **6** wherein the subsequent treatment is a chemical attack or a prolonged high temperature heat treatment.

8. The method of claim **1** which further comprises subjecting the wafer to a stabox process prior to encapsulating the exposed edge of the intermediate layer.

9. A preventive treatment method for a multilayer semiconductor wafer that includes a supporting substrate, at least one intermediate layer and a surface layer in which an intermediate layer has an exposed lateral edge and the wafer is to be subjected to a subsequent treatment, which method comprises annealing the wafer to cause a portion of the surface layer to encapsulate the exposed lateral edge of the intermediate layer to prevent attack on the peripheral edge during the subsequent treatment, wherein the annealing comprises a rapid thermal annealing conducted at a temperature about 1150° C. to 1300° C. for a time of about 1 to 5 minutes to cause the surface layer portion to cover the exposed lateral edge of the intermediate layer.

10. The method of claim **9** wherein the annealing temperature is on the order of about 1200° C. and the annealing time is less than about 3 minutes.

11. The method of claim **9** wherein the annealing is conducted under an atmosphere of hydrogen or argon.

12. A multilayer semiconductor wafer that includes a supporting substrate, at least one intermediate layer having an exposed lateral edge, and a monocrystalline surface layer from a donor wafer, wherein the exposed lateral edge of the intermediate layer is encapsulated with a portion of the monocrystalline surface layer to prevent attack on the peripheral edge during subsequent treatments, wherein the surface layer is made of a monocrystalline material and the exposed lateral edge of the intermediate layer is encapsulated by the monocrystalline material.

13. The wafer of claim **12** in the form of a silicon on insulator structure.

14. A preventive treatment method for a multilayer semiconductor wafer that includes a supporting substrate, at least

one intermediate layer and a surface layer in which an intermediate layer has an exposed lateral edge and the wafer is to be subjected to a subsequent treatment, which method comprises encapsulating the exposed lateral edge of the intermediate layer with a portion of the surface layer to prevent attack on the peripheral edge during the subsequent treatment by heating the wafer using a rapid thermal annealing conducted at a temperature about 1150° C. to 1300° C. for a time of about 1 to 5 minute.

15. The method of claim **14** wherein the annealing temperature is on the order of about 1200° C. and the annealing time is less than about 3 minutes.

minutes

16. The method of claim **14** wherein the annealing is conducted under an atmosphere of hydrogen or argon and the surface layer is made of a monocrystalline material so that the exposed lateral edge of the intermediate layer is encapsulated with the monocrystalline material.

17. The method of claim **14** wherein the subsequent treatment is a chemical attack or a prolonged high temperature heat treatment.

18. The method of claim **14** further comprises subjecting the wafer to a stabox process prior to encapsulating the exposed edge of the intermediate layer.

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